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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/707,249 | 12/01/2003 | Yao Tung Yen | PS-109 | 1248 |

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| EXAMINER |
|---|
| NGUYEN, DANG T |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2824 | |

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/707,249 | YEN, YAO TUNG | |
| | Examiner | Art Unit | |
| | Dang T Nguyen | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-16* is/are allowed.

6)☒ Claim(s) *1,2,4,17 and 18* is/are rejected.

7)☒ Claim(s) *3,5-10,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/01/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

## DETAILED ACTION

1. This action is responsive to the following communications: the Application and the Information Disclosure Statement filed on December 01, 2003.

2. Claims 1 – 20 are pending in this case. Claims 1, 11, and 17 are independent claims.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 1, 2, 4, 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Umemura et al., U.S. Patent No. 6,125,419 – filed June 13,1997.**

**Regarding independent claim 1**, Fig. 3 of Umemura et al. discloses a trace-impedance-matched board comprising: a substrate (Col. 14 lines 10 – 11) containing wiring traces [51a] that include an input trace ending at a first junction [D], a plurality of branch traces (two branch traces Zm at the junction [D]) on the substrate, the plurality of branch traces branching from the first junction to a plurality of end points [#n – 1]; wherein a first equivalent impedance is a reciprocal of a sum of reciprocals of branch impedances of branch traces branching from the first junction in the plurality of branch traces (Fig. 4 disclosing of two parallel impedance 52a and 54a branched at the first junction D; wherein a intrinsic equivalent impedance $Z_{equivalent}$ = 1/(1/80ohm +1/80ohm)

= 40ohm ) wherein an input impedance [Zs] of the input trace [51a] is adjusted to match the first equivalent impedance (Col. 7 lines 36 – 40).

**Regarding dependent claim 2**, Umemura discloses wherein the input impedance is adjusted by enlarging a width of the input trace or a thickness of the input trace (Col. 7 lines 44 – 47).

**Regarding dependent claim 4**, Umemura discloses wherein each branch trace in the plurality of branch traces [Zm] has an impedance within 10 percent of a base impedance Z0 (Zm = 80 ohm); wherein the plurality of branch traces comprises N branch traces (two of Zm branches) that branch form the first junction [D], wherein N is a whole number of at least two (two Zm braches); wherein the input impedance is adjusted to be within 10 percent of Z0/N (Zs = Zm/2 = 40 ohm).

**Regarding independent claim 17**, Fig. 3 of Umemura et al. discloses a module with impedance-matched trace junctions comprising: substrate means (Fig. 11 [7a]) for traces (Fig. 3 [51a, 52a, 54a]) formed on the supporting chips (Fig. 3 [#1 - # n]) driven by wiring substrate means (Fig. 3 [51a, 52a, 54a]); input interconnect means (Fig. 3 [51a] for transmitting a signal (Fig. 3 [12a]) along a wiring trace (Fig. 3 [51a]) to a first junction (Fig. 3 [D]); first branch interconnect means (Fig. 4 [52a]) for connecting the signal to a first chip (Fig. 3[#1]) on the substrate means; second branch interconnect means (Fig. 4 [54a]) for connecting the signal to a second chip (Fig. 3 [#2]) on the substrate means; and first junction means (Fig. 3 [D]), receiving the signal from the input interconnect means (Fig. 4 [51a]), for connecting the signal (Fig. 4 [12a]) to the first branch interconnecting means (Fig. 4 [52a]) and to the second branch interconnect

means (Fig. 4[54a]), the first junction means (Fig. 3 [D]) being a junction of the wiring traces; wherein an input impedance (Fig. 4[Zs =40ohm]) of the input interconnect means (Fig. 4[51a]) matches an equivalent impedance (Fig. 4 [$Z_{equivalent}$ = 1/(1/Zm + 1/Zm) = 1/(1/80 ohm +1/80 ohm) = 40 ohm]) of branch traces driven from the first junction means (Fig. 3 [D]), including the first and second branch interconnect means (Fig. 4 [52a, 54a]), whereby impedance is matched at the first junction means (Fig. 4).

**Regarding dependent claim 18**, Umemura discloses wherein the input impedance is matched to within 20 percent of the equivalent impedance (Fig. 4 discloses Zs is equal to $Z_{equivalent}$ of parallel impedance 52a and 54a, therefore Zs is matched well within 20 percent of $Z_{equivalent}$ )

***Allowable Subject Matter***

4. Claims 3 – 10, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

**With respect to claim 3**, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "wherein a width of the input trace is matched to a sum of widths of branch traces branching from the first junction".

**With respect to claim 5**, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "wherein the input trace is N times wider than each of the branch traces in the plurality of branch traces".

**With respect to claim 9**, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "a trunk branch trace branching from a second junction, receiving a the first junction; signal driven from the input trace, through the first junction to the trunk branch trace; and a plurality of secondary branch traces that branch from the second junction; wherein the second junction outputs a signal to the plurality of secondary branch traces; wherein a second equivalent impedance is a reciprocal of a sum of reciprocals of second secondary branch traces that branch from the second junction in the plurality of secondary branch traces ; wherein a trunk impedance of the trunk branch trace is adjusted to match the second equivalent impedance"

**With respect to claim 10**, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "wherein the input trace carries a true signal of a differential signal; further comprising: a complement input trace ending at a complement junction, the complement input trace carrying a complement signal of the differential signal; a plurality of complement branch traces on the substrate, the plurality of complement branch traces branching from the complement junction to complement endpoints; a plurality of wherein a first complement equivalent impedance is a reciprocal of a sum of reciprocals of complement branch impedances of complement branch traces branching from the complement junction in the plurality of complement branch

traces; wherein a complement input impedance of the complement input trace is adjusted to match the first complement equivalent impedance, whereby the differential signal is carried by a pair of impedance-matched traces".

**With respect to claim 19**, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "wherein a width of the input interconnect means is matched to a sum of widths of branch traces driven from the first junction means, including a first width of the first branch interconnect means and a second width of second branch interconnect means".

**With respect to claim 20**, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "first trunk interconnect means for further distributing the signal from the first junction means, the first trunk interconnect means being a branch trace from the first junction means; third branch interconnect means for connecting the signal to a third chip on the substrate means; fourth branch interconnect means for connecting the signal to a fourth chip on the substrate means; and second junction means, receiving the signal from the first trunk interconnect means, for connecting the signal to the third branch interconnect means and to the fourth branch interconnect means, the second junction means being another junction of the wiring traces; wherein a trunk impedance of the first trunk interconnect means matches a secondary equivalent impedance of secondary branch traces driven from the second junction means, including the third and fourth branch interconnect means, whereby impedance is matched at the second junction means".

6. Claims 11 – 16 are allowed.

**With respect to claim 11**, in addition to other elements in the respective claim, the prior art does not teach or suggest "an impedance-matched module having a third branch line in the plurality of wiring traces; a primary junction connecting an end of the input line to the first branch line, the second branch line, and to the third branch line; wherein a first equivalent impedance is a parallel combination of impedances of branches from the primary junction including a first impedance of the first branch line, a second impedance of the second branch line, and a third impedance of the third branch line; wherein the input line has an input impedance that is matched to the first equivalent impedance by widening or thickening the input line".

***Prior art***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

| | | |
|---|---|---|
| Fan et al. | Patent No. US 6,381,164 B1 | Date of Patent: Apr. 30, 2002 |
| Mellitz et al. | Patent No. 6,078,965 | Date of Patent: Jun. 20, 2000 |
| Sullivan | Patent No. US 6,437,660 B1 | Date of Patent: Aug. 20, 2002 |

***Contact Information***

8. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

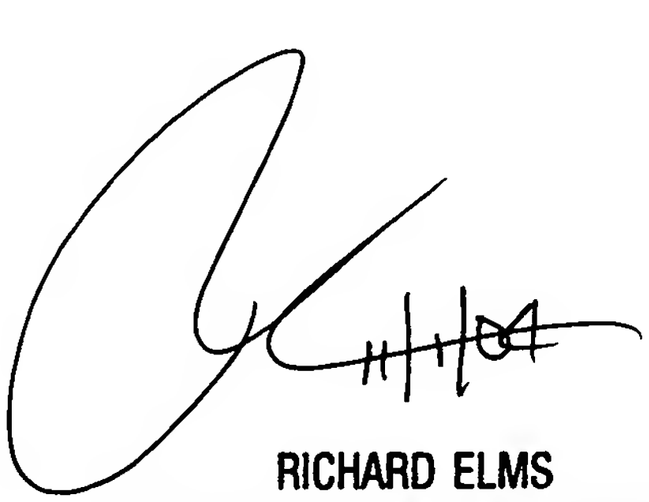
Upon an unsuccessful attempt to contact the examiner, the examiner's

supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 10/25/2004



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